APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,753	12/03/2001	Shoab Ahmad Khan	0037203-7	8281

29484 7590 11/03/2005		EXAMINER
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IRVINE, CA 92604	ART UNIT	PAPER NUMBER
	2136	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/004,753	KHAN ET AL.
	Examiner	Art Unit
	David G. Cervetti	2136

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19-22* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 19-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *8/19/05*.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Applicant's arguments filed August 19, 2005, have been fully considered but they are not persuasive.

2.   Claims 1-17 and 19-22 are pending and have been examined.

Response to Amendment

3.   The objection to the drawings is withdrawn.

4.   The objections to the disclosure and to the abstract of the disclosure are withdrawn.

5.   In response to applicant's arguments, the recitation "a media processor, implemented as a system on a chip, for the processing of media based upon instructions" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Claim Rejections - 35 USC § 102

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7.   Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by

Parameswaran Nair et al. (US Patent Number: 5,724,356, hereinafter

"Parameswaran Nair").

Regarding claim 1, Parameswaran Nair teaches a plurality of processing layers

wherein each processing layer has at least one processing unit, at least one program

memory, and at least one data memory, each of said processing unit, program memory,

and data memory being in communication with one another (column 5, lines 53-67,

column 6, lines 10-20, column 8, lines 48-61); at least one processing unit in at least

one of said processing layers performing line echo cancellation functions on received

data (column 6, lines 1-67); at least one processing unit in at least one of said

processing layers performing encoding or decoding functions on received data (column

6, lines 1-67); and a task scheduler adapted to receive a plurality of tasks from a source

and distributing said tasks to said processing layers (column 25, lines 24-38).

Regarding claim 2, Parameswaran Nair teaches further comprising a direct

memory access controller for handling data transfers, each of said transfers having a

size and a direction, from at least one data memory having an address and a plurality of

external memory units, each having an address (column 19, lines 15-50).

Regarding claim 3, Parameswaran Nair teaches wherein said transfers between

at least one data memory and at least one external memory occur by utilizing the

address of the data memory, the address of the external memory, the size of the

transfer, and the direction of the transfer (column 19, lines 15-50).

Regarding claim 4, Parameswaran Nair teaches wherein the task scheduler is

in communication with an external memory (column 25, lines 24-38, 49-59).

Regarding claim 5, Parameswaran Nair teaches the media processor of claim 1,

further comprising an interface for the receipt and transmission of data and control

signals (column 5, lines 40-65).

8.   **Claims 12-16, 19-22 are rejected under 35 U.S.C. 102(b) as being anticipated**

by Lodenius (US Patent Number: 5,923,761).

Regarding claim 12, Lodenius teaches a plurality of media processors, each of

said media processors having a plurality of processing layers wherein each processing

layer has at least one processing unit, at least one program memory, and at least one

data memory, each of said processing unit, program memory, and data memory being

in communication with one another (column 2, lines 35-67, column 3, lines 1-67, column

4, lines 1-67), wherein at least one processing unit in at least one of said processing

layers performs echo cancellation functions on received data (column 3, lines 1-67,

column 4, lines 1-67), wherein at least one processing unit in at least one of said

processing layers performs encoding or decoding functions on received data (column 3,

lines 1-67), and wherein a task scheduler is adapted to receive a plurality of tasks from

a source and distributing said tasks to the processing layers (column 4, lines 1-67); and

wherein each of said processing layers and task scheduler is implemented as a system

on a chip (column 2, lines 35-67, column 3, lines 1-67, column 4, lines 1-67); a plurality

of packet processors in communication with at least one of said media processors

wherein the packet processor is adapted to packetize processed data (column 2, lines

35-67, column 3, lines 1-67, column 4, lines 1-67); and a host processor in

communication with at least one said packet or media processors (column 3, lines 1-67,

column 4, lines 1-67, column 5, lines 1-67).

Regarding claim 13, Lodenius teaches receiving said media through a data

interface (column 3, lines 1-67, column 4, lines 1-67); scheduling the processing of said

media through a task scheduler adapted to receive a plurality of tasks from a source

and distributing said tasks to a plurality of processing layers (column 4, lines 1-67); and

processing said media in the plurality of processing layers wherein each processing

layer has at least one processing unit, at least one program memory, and at least one

data memory, each of said processing unit, program memory, and data memory being

in communication with one another wherein each of said receiving, scheduling, and

processing steps occurs in a processor implemented as a system on a chip (column 2,

lines 35-67, column 3, lines 1-67, column 4, lines 1-67).

Regarding claim 19, Lodenius teaches a processor for the processing of data

based upon instructions, comprising: a plurality of processing layers wherein each

processing layer has at least one processing unit, at least one program memory, and at

least one data memory, each of said processing unit, program memory, and data

memory being in communication with one another (column 3, lines 1-67, column 4, lines 1-67); and a task scheduler capable of receiving a plurality of tasks from a source and distributing said tasks to the processing layers (column 4, lines 1-67) wherein each of said processing layers and task scheduler is implemented in a single system on a chip (column 3, lines 1-67, column 4, lines 1-67).

Regarding claims 14 and 20, Lodenius teaches performing echo cancellation functions on received data (column 3, lines 1-67, column 4, lines 1-67).

Regarding claims 15 and 21, Lodenius teaches performing encoding or decoding functions on received data (column 3, lines 1-67).

Regarding claim 16, Lodenius teaches wherein the processing step occurs in parallel across multiple processing layers, each of said processing layers having similar processing units (column 2, lines 1-67, column 3, lines 1-67, column 4, lines 1-67).

Regarding claim 22, Lodenius teaches wherein the plurality of processing layers communicate with the task scheduler through a controller interface (column 4, lines 1-67, column 5, lines 1-67).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Parameswaran Nair, and further in view of Chakrabarti et al. (US Patent Number:

6,807,167, hereinafter "Chakrabarti").

Regarding claim 6, Parameswaran Nair does not disclose expressly wherein the

interface comprises a UTOPIA-compatible interface. However, Chakrabarti teaches

wherein the interface comprises a UTOPIA-compatible interface (column 3, lines 5-15).

Therefore, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to use a UTOPIA-compatible interface. One of ordinary skill in

the art would have been motivated to perform such a modification to provide support for

circuit switching and packet switching applications and for supporting multimedia

applications (Chakrabarti, column 1, lines 30-45).

Regarding claim 7, Parameswaran Nair does not disclose expressly wherein the

interface comprises a time division multiplex-compatible interface. However,

Chakrabarti teaches wherein the interface comprises a time division multiplex-

compatible interface (column 3, lines 5-15). The motivation for combining is the same as

that for claim 6 above.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parameswaran Nair, and further in view of Hudepohl et al. (US Patent Number: 6,754,804, hereinafter "Hudepohl").

Regarding claim 8, Parameswaran Nair does not disclose expressly wherein at least one processing layer includes a processing unit performing line echo cancellation functions on received data and a processing unit designed performing encoding or decoding functions on received data and wherein said line echo cancellation and encoding or decoding functions are performed in a pipelined manner. However, Hudepohl teaches wherein at least one processing layer includes a processing unit performing line echo cancellation functions on received data and a processing unit designed performing encoding or decoding functions on received data and wherein said line echo cancellation and encoding or decoding functions are performed in a pipelined manner (column 24, lines 40-60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use systems with multiple processing units and to perform tasks on a pipelined manner. One of ordinary skill in the art would have been motivated to do so because it is well known in the art that utilizing multiple processing units and performing tasks in a pipelined manner increases overall system performance.

Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parameswaran Nair, and further in view of Ehlig et al. (US Patent Number: 6,134,578, hereinafter "Ehlig").

Regarding claim 9, Parameswaran Nair does not disclose expressly wherein the processing unit designed to perform encoding or decoding functions comprises an arithmetic and logic unit, multiply and accumulate unit, barrel shifter, and normalization unit. However, Ehlig teaches a processing unit comprising an arithmetic and logic unit (column 7, lines 37-43), multiply (column 9, lines 5-10) and accumulate unit (column 7, lines 25-35), barrel shifter (column 9, lines 45-65), and normalization unit (column 15, lines 27-41). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use processing units comprising an arithmetic and logic unit, multiply and accumulate unit, barrel shifter, and normalization unit. One of ordinary skill in the art would have been motivated to do so because it provides performance improvement over general purpose microprocessors to allow its use in real-time applications, such as speech and image processing (Ehlig, column 2, lines 1-35).

Regarding claim 10, Parameswaran Nair does not disclose expressly wherein the processing unit additionally performs voice activity detection and tone signaling functions. However, Ehlig teaches wherein the processing unit additionally performs voice activity detection and tone signaling functions (column 26, lines 36-46, column 27, lines 1-15). The motivation for combining is the same as that for claim 9 above.

Regarding claim 11, the combination of Parameswaran Nair and Ehlig teaches the limitations as set forth under claim 10 above. Furthermore, Ehlig teaches wherein the processing unit comprises a plurality of single-cycle multiply and accumulate units

operating with an address generation unit and an instruction decoder (column 18, lines 1-35).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lodenius, and further in view of Hudepohl.

Regarding claim 17, Lodenius does not disclose expressly wherein at least one processing layer includes a processing unit performing echo cancellation functions on received data and a processing unit performing encoding or decoding functions on received data and wherein said echo cancellation and encoding or decoding functions are performed in a pipelined manner. However, Hudepohl teaches wherein at least one processing layer includes a processing unit performing echo cancellation functions on received data and a processing unit performing encoding or decoding functions on received data and wherein said echo cancellation and encoding or decoding functions are performed in a pipelined manner (column 24, lines 40-60). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use systems with multiple processing units and to perform tasks on a pipelined manner. One of ordinary skill in the art would have been motivated to do so because it is well known in the art that utilizing multiple processing units and performing tasks in a pipelined manner increases overall system performance.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David G. Cervetti whose telephone number is (571) 272-5861. The examiner can normally be reached on Monday-Friday 7:00 am - 5:00 pm, off on Wednesday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the
Patent Application Information Retrieval (PAIR) system. Status information for
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